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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,318	04/20/2004	Yoji Asahi	300.1158	4043
21171	7590	03/27/2006	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			TRINH, HOA B	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/827,318

Applicant(s)

ASAHI ET AL.

Examiner

Vikki H. Trinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 09 December 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### Acknowledgement

An amendment filed on 12/09/05 has been considered. Claims 1-8 are pending.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Abe (Pub. No. US 2003/0136577).

Abe discloses, as to claim 1, a semiconductor device substrate comprised of a core substrate 10 (fig. 1) on both surfaces of which interconnect patterns 20 (20a, 20b), 24, 28 (fig. 1) are formed via a resin layer 14 (fig. 1), wherein the core substrate 10 is formed by a material (page 4, Table 1, paragraph [0053]) having a heat expansion coefficient closer to that of a semiconductor chip than those of the main resin layers 14, 22, 26, 30 (fig. 1) and the interconnect patterns 20, 24, 28 (fig. 1) inside the substrate, and a resin layer 30 (fig. 1, page 3, paragraph [0045] and page 4, paragraph [0063], Table 1) forming an outermost layer of the substrate 10 on each of the main surfaces thereof of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers 14, or 22 or 26 (fig. 1) in the substrate 10, thereby preventing cracking, deformation, and other problems arising

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in the substrate due to the thermal stress occurring between the core substrate and the inner resin layers in the substrate and interconnect patterns in the substrate.

Note: the resin layers 14, 22, 26, 30 (fig. 1) can be selected among the disclosed group of materials (page 4, [0063]) so as to provide the outermost layer with the higher strength and elongation than the inner layer.

As to claims 2, and 6, Abe further discloses that a resin layer 26 (fig. 1, page 3, paragraph [0045] and page 4, paragraph [0063], Table 1) under the resin layer 30 (fig. 1) forming the outermost layer of the substrate 10 is made of a resin material having at least one of a higher strength and higher elongation than the resin material of the resin layer 14 or 22 (fig. 1) used further inside the substrate 10 (fig. 1).

As to claims 3, and 7, Abe further discloses that the resin material forming the outermost layer 30 has a fracture strength of at least 90 Mpa and elongation of at least 10%. (See page 4, paragraph [0063], Table 1) Note: example of such material is a polyimide resin.

As to claims 4, and 8, Abe discloses the resin material forming the outermost layer 30 (fig. 1) has a fracture strength of at least 90 Mpa and elongation of at least 10%. (See page 4, paragraph [0063], Table 1) Note: example of such material is a polyimide resin.

As to claim 5, Abe discloses a semiconductor device substrate comprised of a core substrate 10 (fig. 1) on both surfaces of which interconnect patterns 20 (20a, 20b), 24, 28 (fig. 1) are formed via a resin layer 14 (fig. 1), wherein the core substrate 10 is formed by a material (page 4, Table 1, paragraph [0053]) having a heat expansion coefficient closer to that of a semiconductor chip than those of the main resin layers 14, 22, 26, 30 (fig. 1) and the interconnect patterns 20, 24, 28 (fig. 1) inside the substrate, and a resin layer 30 (fig. 1, page 3,

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paragraph [0045] and page 4, paragraph [0063], Table 1) forming an outermost layer of the substrate 10 on each of the opposite main surfaces (fig. 1) thereof of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers 14, or 22 or 26 (fig. 1) in the substrate 10.

### ***Response to Arguments***

3. Applicant's arguments filed 12/09/05 have been fully considered but they are not persuasive.

In the remarks, applicants contend that Abe does not teach resin layers on main surfaces of the core substrate. On the contrary, Abe does disclose in figure 1 the resin layers on the main surface of the substrate. Additionally, the materials (polyimide based and/or epoxy based) select for the resin layers in Table 1 of Abe have the same characteristics as those disclosed on page 8 of the present invention application, because they are essentially the same materials. Furthermore, applicants are wrong to state that Abe's invention does not have any relevancy to a semiconductor device in accordance with the present invention, because Abe teaches on page 1, [0012], a circuit board for mounting semiconductor elements, thereby being in the same field of endeavors as the present invention.

For the foregoing reasons, the examiner maintains the rejection.

### **Conclusion**

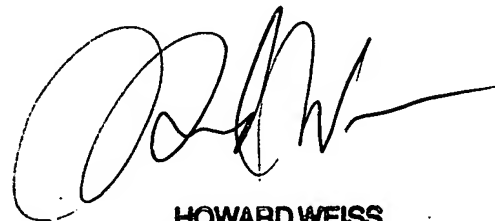
Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If

attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see if you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,  
Patent Examiner  
AU 2814



**HOWARD WEISS  
PRIMARY EXAMINER**